Claims

1. through 19. (Cancelled)

20. (New) A method for synthesizing a linear finite state machine (LFSM), comprising:

receiving an original LFSM circuit, the original LFSM circuit comprising a plurality of memory elements and linear logic gates coupled between some of the memory elements, the original LFSM circuit further comprising one or more feedback connections, each feedback connection originating at a respective source tap and ending at a respective destination tap; and

modifying the original linear finite state machine (LFSM) circuit by moving the respective source tap and the respective destination tap of a selected one of the feedback connections in a same direction across a same number of memory elements, thereby creating a modified LFSM circuit.

21. (New) The method of claim 20, wherein the modified LFSM circuit is capable of providing the same output sequence as the original LFSM circuit.

22. (New) The method of claim 20, wherein the act of modifying reduces the length of a feedback connection line associated with the selected feedback connection.

23. (New) The method of claim 20, wherein the act of modifying reduces levels of linear logic in the original LFSM circuit.

24. (New) The method of claim 20, wherein the act of modifying reduces internal fan-out in the original LFSM circuit.

25. (New) The method of claim 20, wherein the act of modifying further comprises adding a new feedback line for the selected feedback connection if the respective source tap or the respective destination tap of the selected feedback connection is moved across a source or destination tap of another feedback connection.

26. (New) A computer-readable medium storing the modified LFSM circuit created by the method of claim 20.

27. (New) A computer-readable medium comprising computer-readable instructions for causing a computer to perform the method of claim 20.

28. (New) A method for synthesizing a linear finite state machine (LFSM), comprising:

obtaining an original LFSM circuit, the original LFSM circuit comprising a plurality of memory elements and linear logic gates coupled between some of the memory elements, the original LFSM circuit further comprising a feedback connection line originating at a source tap coupled to an output of one of the memory elements and ending at a destination tap coupled to an input of another of the memory elements; and

reducing the length of the feedback connection line by shifting the source tap and the destination tap across a number of the memory elements, thereby transforming the original LFSM circuit into a modified LFSM circuit that is capable of providing the same output sequence as the original LFSM circuit.

29. (New) The method of claim 28, wherein the source tap and the destination tap are shifted in the same direction.

30. (New) The method of claim 28, wherein the source tap is a source tap for one or more additional destination taps, and wherein the act of shifting further comprises splitting the source tap into at least two source taps, one of the at least two source taps being the source tap shifted across the number of memory elements.

31. (New) The method of claim 28, further comprising adding a new feedback line if the source tap or the destination tap is shifted across a source or destination tap of another feedback connection line.

32. (New) The method of claim 31, wherein the new feedback line creates the functionality of the original LFSM circuit in the modified LFSM circuit.

33. (New) The method of claim 28, wherein the fan-out of the feedback connection line is two or less.

34. (New) The method of claim 28, wherein the destination tap comprises an XOR or XNOR gate.

35. (New) A computer-readable medium storing the modified LFSM created by the method of claim 28.

36. (New) A computer-readable medium comprising computer-readable instructions for causing a computer to perform the method of claim 28.

37. (New) A method for synthesizing a linear finite state machine (LFSM), comprising:

a step for obtaining an original LFSM circuit, the original LFSM circuit comprising a plurality of memory elements and linear logic gates coupled between some of the memory elements, the original LFSM circuit further comprising a feedback connection line originating at a source tap coupled to an output of one of the memory elements and ending at a destination tap coupled to an input of another of the memory elements; and

a step for reducing the length of the feedback connection line by shifting the source tap and the destination tap across a number of the memory elements, thereby transforming the original LFSM circuit into a modified LFSM circuit that is capable of providing the same output sequence as the original LFSM circuit.

38. (New) The method of claim 37, wherein the source tap is a source tap for one or more additional destination taps, and wherein the step of shifting further comprises a step for splitting the source into at least two source taps, one of the at least two source taps being the source tap shifted across the number of memory elements.

39. (New) The method of claim 37, further comprising a step for adding a new feedback line if the source tap or the destination tap is shifted across a source or destination tap of another feedback connection line.